AMENDMENTS TO THE SPECIFICATION

Please amend the Title on page 1 as follows:

CMOS ~~SOLID STATE~~ IMAGING DEVICE FOR AMPLIFYING AND FETCHING SIGNAL CHARGE

Please replace the paragraph beginning at page 27, line 8, with the following rewritten paragraph:

Furthermore, in the CMOS image sensor shown in FIG. 1, an OR circuit 12 is newly provided wherein a variable electronic shutter pulse signal ~~ΦESPB~~ ΦESPA is appropriately supplied as an external input pulse signal. To the OR circuit 12, an electronic shutter pulse signal ΦESPB having a fixed phase which signal is generated at the timing generation circuit 10 is input together with an electronic shutter pulse signal ~~ΦESPB~~ ΦESPA having a variable phase. The electronic shutter pulse signal ΦESREAD generated through the synthesis of the variable electronic shutter pulse signal ~~ΦESPB~~ ΦESPA and the fixed electronic shutter pulse signal ~~ΦESPA~~ ΦESPB in the OR circuit 12 is output to the pulse selector. Incidentally, in this CMOS image sensor, the variable electronic shutter pulse signal ΦESPA is supplied in the horizontal effective scanning period when needed while the fixed electronic shutter pulse signal ΦESPB is constantly generated in the horizontal blanking period.

Please replace the paragraph beginning at page 28, line 27, with the following rewritten paragraph:

Here, in FIG. 2B, the electric charge accumulation time is controlled to less than 1H (a horizontal cycle) by supplying the variable electronic shutter pulse signal ΦESPA in the horizontal effective scanning period with the result that the electric charge accumulation time

can be further variably controlled by changing the phase of the variable electronic shutter pulse signal Φ ESPA. On the other hand, in FIGS. 2A and 2C, the signal accumulation timing is set with the fixed electronic shutter pulse signal ~~Φ ESPA~~ Φ ESPB. Thus, the variable electronic shutter pulse signal Φ ESPA is constantly on an "L" level and is not sufficiently used.

Please replace the paragraph beginning at page 36, line 24, with the following rewritten paragraph:

Incidentally, in this case, as shown in FIG. 4, the phase difference between the first time reset pulse signal Φ RESET and the fixed electronic shutter pulse signal Φ ESPB and the phase difference between the second time reset pulse signal Φ RESET and the signal reading pulse signal Φ ROREAD are set to approximately the same level. Furthermore, in the case where the external input pulse signal is input at the timing shown in FIG. 2C is supplied as well, the electronic shutter pulse signal Φ ESREAD is supplied with the vertical selection pulse signal Φ ADRES to the outside of the period in which the signal of the vertical selection line 6 of the line to be selected is activated lest the accumulation electric load discharged from the photodiode be read to the vertical signal VLIN. Specifically, the variable electronic shutter pulse signal ~~Φ ESPB~~ Φ ESPA is supplied to the horizontal effective scanning period, so that the fixed shutter pulse signal Φ ESPB supplied from the timing generation circuit in the horizontal blanking period is controlled so as to fall prior to the start-up of the vertical selection pulse signal Φ ADRES.

Please replace the paragraph beginning at page 39, line 6, with the following rewritten paragraph:

The electric charge accumulation time of the photodiode here extends from the reading drive signal Φ READi output in the horizontal effective scanning period on the basis of the variable electronic shutter pulse signal ~~Φ ESPB~~ Φ ESPA up to the signal reading timing in the horizontal blanking period subsequent to this horizontal effective scanning period, so that 1H (horizontal cycle) can be more shortened. Besides, the supply timing of the variable electronic shutter pulse signal ~~Φ ESPB~~ Φ ESPA is rendered variable in a period immediately after the start of the horizontal effective scanning period up to immediately before the end of the horizontal effective scanning time, so that the electric charge accumulation time can be freely set approximately within the scope of not less than the horizontal blanking period and less than 1H (horizontal cycle).

Please replace the paragraph beginning at page 52, line 3, with the following rewritten paragraph:

Incidentally, in FIG. 12, on the basis of the control of the count signal ADCK from the timing generation circuit 10, the operation of the A/D conversion circuit and the reference signal generation circuit is temporarily suspended all through the process before and after the input of the variable electronic shutter pulse signal Φ ESPA ~~on the basis of the variable electronic shutter pulse signal Φ ESPA~~. This is because it is thought that when the variable electronic shutter pulse signal Φ ESPA is input in the horizontal effective scanning period, there is a fear that fluctuation in the power source voltage and in the ground voltage is generated, so that noise might jump into the analog signal.